

67,200-377; TSMC 00-723
Serial Number 10/632,379

LISTING OF THE CLAIMS

The following Listing of the Claims replaces all prior listings of the claims within this application.

Claims 1, 3-5, 8, 10-12 and 14 are amended.

1. (currently amended) A field effect transistor (FET) device comprising ~~a surface of the channel region being corrugated.~~

a semiconductor substrate;

a gate electrode formed over the semiconductor substrate and covering a channel region within the semiconductor substrate; and

a pair of source/drain regions formed within the semiconductor substrate and separated by the channel region within the semiconductor substrate, wherein at least one of:

an interface of the channel region covered by the gate electrode; and

an upper surface of the gate electrode, is corrugated.

2. (original) The field effect transistor (FET) device of claim 1 wherein the field effect transistor (FET) device is selected from the group consisting of metal oxide semiconductor field effect transistor (MOSFET) devices and metal semiconductor field effect transistor (MESFET) devices.

3. (currently amended) The field effect transistor (FET) device of claim 1 wherein the at least one of:

the interface of the channel region covered by the gate electrode; and

the upper surface of the channel region gate electrode, is corrugated with a peak-to-peak longitudinal periodicity of from about 0.02 to about 0.4 microns and a peak-to-valley vertical depth of from about 100 to about 1000 angstroms.

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4. (currently amended) ~~The~~ A field effect transistor (FET) device comprising: of claim 1 wherein only the interface of the channel region covered by the gate electrode is corrugated.

a semiconductor substrate;

a gate electrode formed over the semiconductor substrate and covering a channel region within the semiconductor substrate; and

a pair of source/drain regions formed within the semiconductor substrate and separated by the channel region within the semiconductor substrate, wherein an interface of the channel region covered by the gate electrode is corrugated.

5. (currently amended) ~~The~~ A field effect transistor (FET) device comprising: of claim 1 wherein only the upper surface of the gate electrode is corrugated.

a semiconductor substrate;

a gate electrode formed over the semiconductor substrate and covering a channel region within the semiconductor substrate; and

a pair of source/drain regions formed within the semiconductor substrate and separated by the channel region within the semiconductor substrate, wherein an upper surface of the gate electrode is corrugated.

6. (original) The field effect transistor (FET) device of claim 1 wherein both the interface of the channel region covered by the gate electrode and the upper surface of the gate electrode are corrugated.

7. (original) The field effect transistor (FET) device of claim 1 wherein the gate electrode is formed to a thickness of from about 500 to about 2000 angstroms.

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8. (currently amended) A method for forming a field effect transistor (FET) device comprising:

providing a semiconductor substrate;

forming over the semiconductor substrate and covering a channel region within the semiconductor substrate a gate electrode; and

forming within the semiconductor substrate and separated by the channel region within the semiconductor substrate a pair of source/drain regions, wherein at least one of:

an interface of the channel region covered by the gate electrode; and

an upper surface of the channel-region gate electrode, is corrugated.

9. (original) The method of claim 8 wherein the field effect transistor (FET) device is selected from the group consisting of metal oxide semiconductor field effect transistor (MOSFET) devices and metal semiconductor field effect transistor (MESFET) devices.

10. (currently amended) The method of claim 8 wherein the at least one of:

the interface of the channel region covered by the gate electrode; and

the upper surface of the gate electrode, is corrugated with a peak-to-peak longitudinal periodicity of from about 0.02 to about 0.04 0.4 microns and a peak-to-valley vertical depth of from about 100 to about 1000 angstroms.

11. (currently amended) ~~The method of claim 8 wherein only the interface of the channel region covered by the gate electrode is corrugated.~~

A method for forming a field effect transistor (FET) device comprising:

providing a semiconductor substrate;

forming over the semiconductor substrate and covering a channel region within the semiconductor substrate a gate electrode; and

forming within the semiconductor substrate and separated by the channel region within the semiconductor substrate a pair of source/drain regions, wherein an interface of the channel region covered by the gate electrode is corrugated.

12. (currently amended) ~~The method of claim 8 wherein only the upper surface of the gate electrode is corrugated.~~

A method for forming a field effect transistor (FET) device comprising:

providing a semiconductor substrate;

forming over the semiconductor substrate and covering a channel region within the semiconductor substrate a gate electrode; and

forming within the semiconductor substrate and separated by the channel region within the semiconductor substrate a pair of source/drain regions, wherein an upper surface of the gate electrode is corrugated.

13. (original) The method of claim 8 wherein both the interface of the channel region covered by the gate electrode and the upper surface of the gate electrode are corrugated.

14. (currently amended) The method of claim 8 wherein the gate electrode is formed to a thickness of from about 600 to about 200 500 to about 2000 angstroms.